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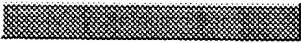
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S99	125	S93 and (profil\$3 with (simulat\$3 or bus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S100	7	S95 and S99	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S101	446	S94 or S95 or S96 or S97 or S98 or S99 or S100	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S102	131	S93 and (bus near2 (traffic or performance or "data transfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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US 6349392 B1	Devices, systems and methods for mode driven stops	20020219 714/30
US 6339836 B1	Automated design partitioning	20020115 716/5
US 6336087 B1	Method and apparatus for gate-level simulation of synthesized register transfer level design wi	20020101 703/15
US 6324678 B1	Method and system for creating and validating low level description of electronic design	20011127 716/18
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120 716/6
US 6314552 B1	Electronic design creation through architectural exploration	20011106 716/18
US 6311310 B1	Method and apparatus for wiring integrated circuits with multiple power buses based on perfor	20011030 703/18
US 6311147 B1	Integrated circuit power net analysis	20011030 703/14
US 6311146 B1	Circuit simulation with improved circuit partitioning	20011016 716/18
US 6305006 B1	Generating candidate architectures for an architectural exploration based electronic design cr	20011016 703/4
US 6304834 B1	Method and apparatus for semiconductor device simulation with linearly changing quasi-fermi p	20010925 708/402
US 6295546 B1	Method and apparatus for eliminating the transpose buffer during a decomposed forward or in	20010925 703/15
US 6295517 B1	Method and apparatus for adaptively or selectively choosing event-triggered cycle-based simul	20010918 382/239
US 6292589 B1	Method for choosing rate control parameters in motion-compensated transform-based picture	20010904 703/2
US 6285970 B1	Computer simulation method of silicon oxidation	20010807 703/13
US 6272451 B1	Software tool to allow field programmable system level devices	20010717 716/18
US 6263484 B1	Prototyping system and a method of operating the same	20010529 703/15
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US 6240375 B1	Method of simulating an integrated circuit for error correction in a configuration model, and a c	20010522 701/300
US 6236940 B1	Display monitor for golf cart yardage and information system	20010522 342/357.13
US 6236360 B1	Golf course yardage and information system	20010515 703/14
US 6233540 B1	Design environment and a method for generating an implementable description of a digital sys	20010515 382/260
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US 6212493 B1	Profile directed simulation used to target time-critical crossproducts during random vector test	20010403 703/12
US 6212487 B1	Method and apparatus of establishing a region to be made amorphous	20010327 703/16
US 6208954 B1	Method for scheduling event sequences	20010227 716/20
US 6195790 B1	Electrical parameter evaluation system, electrical parameter evaluation method, and computer	20010227 235/380
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US 6191663 B1	Echo reduction on bit-serial, multi-drop bus	20010123 714/739
US 6178533 B1	Method and system for design verification	20010109 703/2
US 6173240 B1	Multidimensional uncertainty analysis	20001226 711/149
US 6167491 A	High performance digital electronic system architecture and memory circuit therefor	20001121 257/777
US 6150724 A	Multi-chip semiconductor device and method for making the device by using multiple flip chip i	20001017 703/27
US 6134516 A	Simulation server system and method	20001003 711/212
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US 6085336 A	Data processing devices, systems and methods with mode driven stops	20000704 714/30
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US 6038383 A	Method and apparatus for determining signal line interconnect widths to ensure electromigration	20000314 716/5
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